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ABSTRACT

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Research included the establishment of electrical and optical characterization facilities specifically designed for the study of high resistivity materials and their effects on devices. We have made advances in several areas including low frequency current oscillations, analysis of multiple exponential signals for Deep Level Transient Spectroscopy (DLTS), imaging of deep level domains using voltage contrast in a scanning electron microscope (SEM), surface stability of various passivation techniques and one dimensional, steady state and transient numerical simulations of semi-insulating GaAs transport properties. Additionally we discovered the chaotic properties of the low frequency oscillations.

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Deep Traps and Sidegating in GaAs Devices

George N. Maracas
and
David A. Johnson

July 15, 1989

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D.A. Johnson, G.N. Maracas, R. Puechner, K. Shiralagi, S. Myhajlenko, J. Edwards, H. Goronkin, "Observations of Domains in Semi-insulating GaAs by Voltage Contrast in an SEM," Workshop on Compound Semiconductor Microwave Materials and Devices, Hilton Head, SC, February 1987

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A.Mirchandani, G.R.L. Sohie and G.N. Maracas, "Estimation of time constants of multiple exponentials in noise," International Conference on Acoustics, Speech and Signal Processing, Dallas, TX 1987

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G.N. Maracas, "Conduction Properties of Semi-insulating GaAs," North Carolina State University, Raleigh, NC, March 1988 (invited talk)

G.R.L. Sohie and G.N. Maracas, "Classification of Nonstationarities Using Orthogonal Polynomial Theory," Princeton Conference on Information Sciences and Systems., Princeton, NJ, March 1988

D.A. Johnson, R.A. Puechner, N.S. Kang, K. Wadhera, G.N. Maracas and D.K. Schroder "Electrical and optical evaluation of passivated GaAs surface recombination velocity reduction and fermi level unpinning in GaAs," 1988 GaAs and Related Compounds, Atlanta GA, Sept. 1988

H. Goronkin, G.N. Maracas and P. Fejes, "Effect of Au-GaAs reactions on GaAs FET DC parameters" 1988 GaAs and Related Compounds, Atlanta GA, Sept. 1988

G.N. Maracas, "Electrical Properties of Semi-insulating GaAs for Integrated Circuits," American Vacuum Society Conference, Phoenix, AZ February 1987

D.A. Johnson, "Imaging of Deep Level Domains by Voltage Contrast," MOTOROLA CSTC, June 1987

<u>8 Scientific personnel supported by this project and degrees awarded during this reporting period:</u>

George N. Maracas, Associate Professor E&CE, Principal investigator

Guy L. Sohie, Assistant Professor E&CE, Co-principal Investigator
David A. Johnson, Conduction Mechanisms in Semi-insulating GaAs, PhD Thesis, Arizona State University, May 1989.
Kapil Wadhera, GaAs Surface Passivation and Insulating Buffer Layers, MS Thesis, Arizona State University, May 1989.
Rashid Alameh, Analysis of Multi-exponential Signals in Noise and their Application in Deep Level Transient Spectroscopy, MS Thesis, Arizona State University, December 1988.
Arun Mirchandani, Accurate Estimation of Real Decaying Exponentials in Noise, MS Thesis, Arizona State University, Aug. 1987.

9 Review of research under ARO program

1 Abstract

This is the final technical report for ARO contract DAAL03-86-K-0070. In the report we describe our progress in the areas of semi-insulating GaAs conduction mechanisms and how they apply to the phenomena of sidegating and backgating in GaAs based devices. The experimental and theoretical program evolved into a highly collaborative effort between industry and university with several joint publications resulting. The sidegating/backgating problem has finally been acknowledged as can be seen by the recent creation of a highly interactive workshop dedicated to such effects.

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We have initiated and developed several industrial interactions in the areas of III-V device instabilities and semi-insulating GaAs material characterization. The collaborations are with MOTOROLA Phoenix Corporate Research Lab (PCRL), Spectrum Technologies, MIT Lincoln Laboratory and Hewlett-Packard (HP) Santa Rosa. DARPA and AFOSR have also supplied us with substrates for evaluation.

2 Introduction

This research has involved an experimental and theoretical assessment of conduction mechanisms in semi-insulating (SI) gallium arsenide (GaAs). Special attention has been given to the phenomenon of low frequency current oscillations (LFOs) because they can be used to gain insight into deep level behavior under applied electric fields comparable to those found in GaAs integrated circuits.

There are various parasitic effects which are inherent to the GaAs system. At the single device level these include charge storage effects due to surface states and traps at the channel-substrate interface. Fig. 1. schematically shows the space charge regions in a GaAs MESFET. There is a Schottky barrier induced depletion region under the gate and surface potential induced depletion between the gate and drain and the gate and source. The depletion at the exposed surface between the gate/drain and gate/source is caused by a high density of native surface states which fixes the Fermi level at approximately 0.8 eV below the conduction band in n-type material. Without proper surface passivation, the surface depletion can be a function of bias and environment, thus altering the surface state occupancy and interacting with channel free carriers to produce various transient effects[1] . There is also a space charge region at the channel-substrate interface. Electrons in the highly doped channel can be injected into the semi-insulating substrate where they are trapped by EL2 centers. The EL2 centers are positively charged when empty and just compensate the negative charge of background shallow impurities (eg. carbon, iron, etc.) in the substrate. When the electrons from the channel spill into the substrate and are trapped, the charge from the ionized shallow acceptors is no longer

compensated and produces a net negative charge in the substrate which balances the net positive charge due to ionized shallow donors in the channel. If a negative charge is placed on a backgate (between the surface and a back side contact), as shown in Fig. 1, the channel/substrate space charge region is reverse biased and increases in width. This will in turn cause a decrease in the current flowing through the MESFET. This decrease in drain/source current due to a negative bias on a sidegate or backgate is referred to as backgating. Also, since the compensating traps in the substrate are deep (approximately E_C - 0.8 eV), various slow transient effects are observed due to the filling and emptying of these levels as the operating point and temperature of the MESFET change.

The second category of parasitic effects which can adversely affect the behavior of GaAs ICs is electrical coupling among devices on a chip. These parasitics will increase as the circuit density increases. Fig. 2 illustrates the various mechanisms by which coupling can occur between adjacent devices. In general, interaction between devices can occur through current leakage and potential interactions. These are commonly referred to as sidegating and backgating effects[2,3]. Sidegating occurs when current flows from one device, through the substrate or the surface and into the channel of another device. This current exists because of the finite resistivity of SI GaAs. In fact, reasonably high currents (≤ 1 mA) can flow through the substrate due to surface conduction or space charge limited transport. Often proton or oxygen isolation is used to further isolate devices and reduce the effects of sidegating and backgating[4,5,6]. It is seen that ion implantation does not completely eliminate the effects. Some technologies even utilize p-type guard rings[7] around devices. Epitaxial methods have been proposed to reduce these parasitic effects such as using p-type or highly resistive low temperature MBE buffer layers[8].

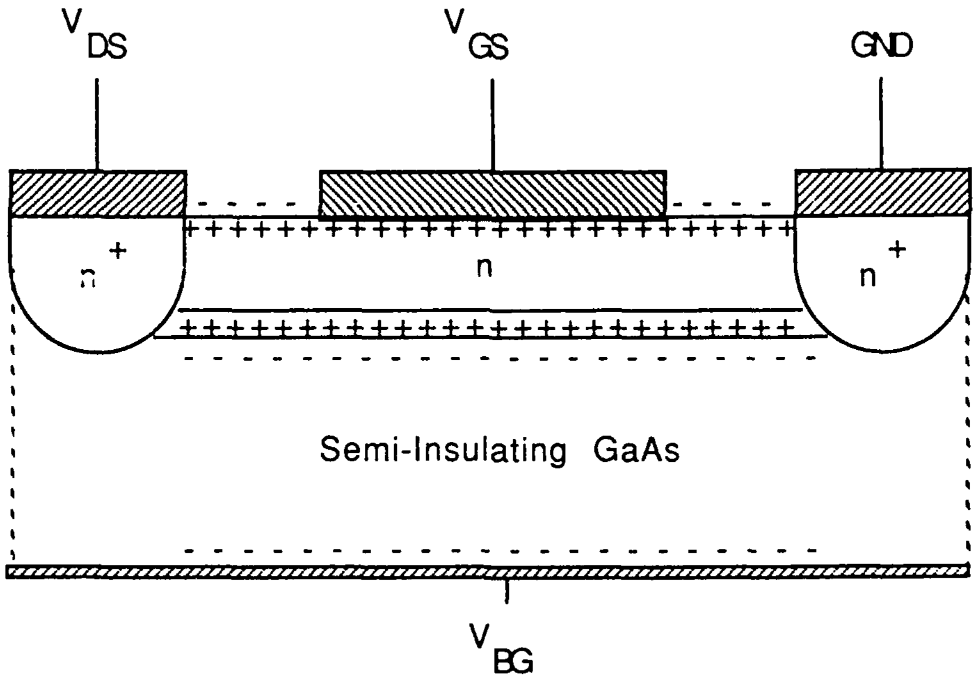

Figure 1. GaAs MESFET showing surface and channel/interface space charge regions and backgating.

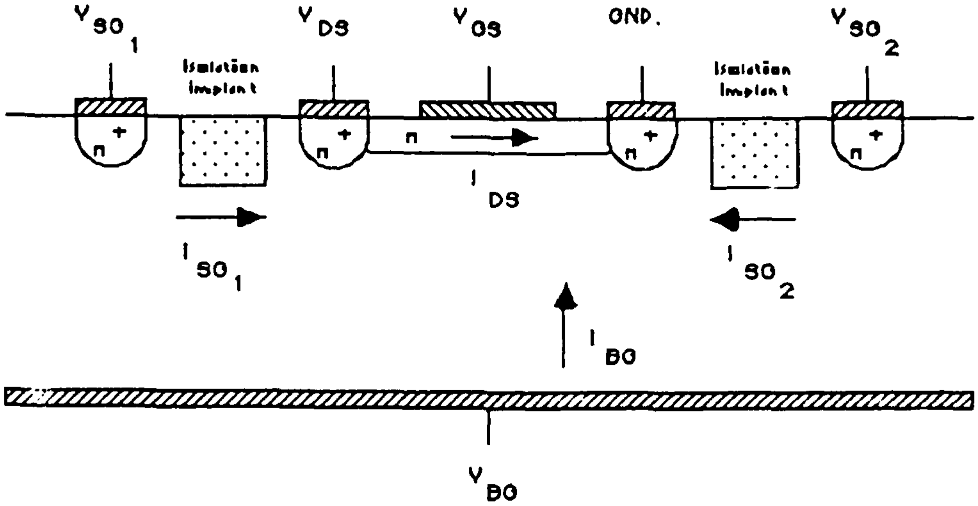

Figure 2. GaAs MESFET sidegating and backgating.

The most successful to date has been the low temperature MBE buffer layer and is presently the topic of much investigation. A complicating factor in trying to compare the various methods is that all of the aforementioned effects vary with circuit geometry, density, device type, and substrate type. In particular, coupling from p-type or Schottky contacts to n-type channels is much different than the coupling from n-type ohmic contacts.

The behavior observed for p-i-n structures, where the insulating layer is highly compensated SI GaAs, is quite different from the behavior observed in n-i-n structures both in terms of noise and the current-voltage (I-V) characteristics.

Finally, low frequency current oscillations (LFOs) have been observed in LEC SI GaAs resistor structures[9] . The LFOs can potentially be a major noise source in GaAs integrated circuits[10] as well as causing instability in the I-V characteristics of discrete devices[11]. The LFOs can occur by more than one mechanism depending on whether the coupling is between an n-type contact and the n-type channel of a MESFET or between a p-type or Schottky contact and the MESFET channel. For an n-type sidegate we will argue that the oscillations are caused by field enhanced capture of electrons by the deep level EL2[12]. For a p-type sidegate, the oscillations are caused by two carrier injection into the SI GaAs[13,14,15]. In general, the oscillations caused by p-type or Schottky sidegates occur at higher frequencies than the corresponding oscillations for n-type sidegates. In both cases, the current oscillations can affect the performance of the individual devices by modulating the width of the channel/substrate space charge region or by coupling currents directly into the MESFET channel.

Therefore, high quality SI GaAs substrates, and a thorough understanding of the conduction properties of the substrates, are required to commercially utilize the advantages offered by the GaAs material system[16]. The substrate requirements include large diameter, high electrical property uniformity, low dislocation density, high resistivity, and thermal stability.

3 Scope of Research

A detailed understanding of the bulk and surface properties of SI GaAs is very important in the efficient development of high packing density GaAs ICs. Our research efforts were directed toward developing a detailed understanding of these coupling mechanisms. Special attention has been given to the low frequency oscillations, the possibility of using these oscillations to develop a simple procedure for evaluating the quality of undoped SI substrates, and a theoretical model which describes the low frequency oscillations in terms of field enhanced trapping by the deep level EL2.

The major research accomplishments in this project are:

a) An automated electrical and optical characterization laboratory specifically designed to characterize SI GaAs material and devices has been established.

b) A new electrical measurement technique (named Deep Level Domain Spectroscopy (DLDS)) to specifically study semi-insulating GaAs substrates has been developed. Using this technique, we have studied the thermionic nature of the LFOs for various sample spacings and substrate types.

c) Two new methods of deconvoluting multiple exponential signals were developed to analyze Deep Level Transient Spectroscopy (DLTS) data. One method has resolved multiple exponentials in noise better than any other previous method.

d) A novel application of the voltage contrast mode of an SEM was used to directly image and measure (for the first time), domain motion in LEC GaAs and dislocation free GaAs:In samples. Several videotapes showing the behavior as a function of voltage and geometry have been used to explain the long-observed LFO current waveforms and settle a controversy of device coupling mechanisms.

e) A study has been undertaken to determine the importance of different surface preparations on the observed conduction and noise phenomena in SI GaAs. Correlation of surface fermi level pinning/unpinning with long term device stability has been made.

f) A 1-D steady state simulation has been developed to describe the electric field, charge, and free carrier concentration in a dipole domain caused by field enhanced trapping of electrons by EL2.

g) A full 1-D transient numerical simulation to describe both the conduction and noise properties for n-i-n, p-i-n, and p-i-p SI GaAs resistor structures has been developed. Good qualitative agreement with experimental data has been obtained.

h) The thermal, geometrical, and surface dependence of the trap filled limited voltage (V_{TH}) has been investigated.

i) The chaotic nature of the low frequency current oscillations in SI GaAs was observed and studied for the first time.

4 Industry Affiliations

a. p-i-n, n-i-n Sidegating Structures (Motorola Inc)

Various n-i-n and p-i-n structures have been and are being fabricated by Motorola on several different SI substrates including some substrates by the new vertical gradient freeze method. Samples also included a study of different isolation implants. These samples are part of a strong continuing collaboration with Motorola. The p-i-n structures will allow us to further our investigations of two carrier phenomena in SI GaAs and to understand the differences to be expected for isolation of n-i-n and p-i-n structures.

b. Low Pressure LEC (Spectrum Technology)

We have been involved in the characterization of low pressure LEC material by Hall effect, photoluminescence, thermally stimulated current, photo-induced transient spectroscopy, and deep level transient spectroscopy. Efforts have been directed toward correlating the presence of defects and impurities with the semi insulating properties of the substrates.

c. Low Temperature MBE Buffer Layers (MIT Lincoln Labs)

A collaboration with MIT Lincoln Laboratory has been established where we are characterizing the sidegating behavior of MBE GaAs buffer layers grown at low temperatures. These structures exhibit essentially no sidegating/backgating behavior. A considerable amount of effort is being dedicated to understand the buffer layer's properties and behavior in devices. At the present time, it is believed that the buffer material is high arsenic, non-stoichiometric GaAs with As precipitates. We are in the process of preparing a manuscript describing its temperature stability.

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5 Other

The problem of deep trap effects on GaAs device stability has drawn so much interest that a workshop on this subject has been organized. The "Workshop on Device Instabilities due to Deep Traps" was held during the last week of April in Sedona, Arizona. The workshop addressed the theoretical and experimental aspects of this problem. The industrial, government and university participants were extremely open in the discussion of problems encountered and also to their solutions.